FCT Assembly LEADERS IN TECHNOLOGY	**Fine Line Stencil Root Cause Analysis Report**	**Rev:** A	**Document no:** **RootCause**

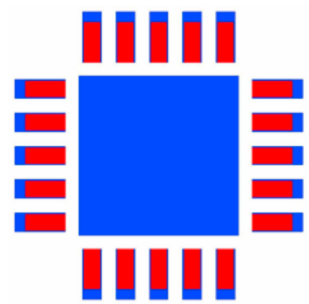
Problem Description:

SMT component U5 QFN 20-pin is having insufficient solder volume at reflow.

Top
QFN 20-pin

Root Cause:

QFN



QFN 20-Pin
(red: termination, blue: SMT pad)

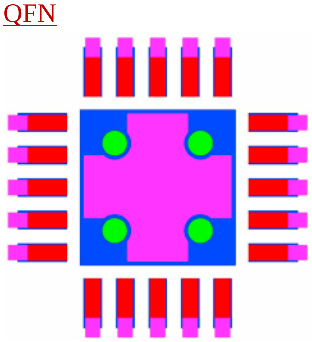
For leadless components, the terminal should cover 90%-100% of the SMT pad on the printed circuit board. On this assembly, the QFN covers 79% (terminal length is 0.0236" and SMT pad length is 0.0299") of the SMT pad. The root cause of the insufficient solder volume is a result of too much surface area for the solder to wet to with enough left over to form an acceptable solder joint.

On leadless components, solder will uniformly wet to the surfaces of the terminal and SMT pad. When the terminal is 90%-100% of the SMT pad, solder is shared between the two surfaces. When the SMT pad is longer than the terminal, it creates surface area that is not shared between the two surfaces. Solder will be pulled from the joint during reflow to cover the additional surface area and the result is insufficient solder volume at the terminal.

There are many assemblies where SMT pads are lengthened on leadless components to aid in the inspection process or provide SMT pad area for rework. Unfortunately, lengthening the SMT pad creates rework. In some cases, the component specifications provide recommended land pad designs that are incorrect, based on thermal mass and the amount of surface area that has to be covered by solder.

Recommendation:

QFN



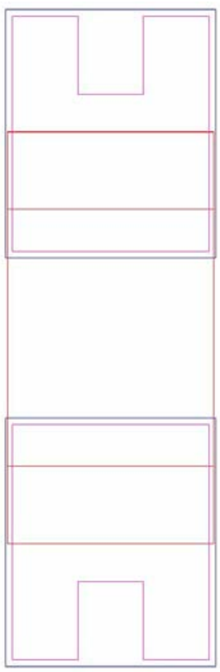
To eliminate the insufficient solder problems with the QFN component, the volume of solder printed must be increased, given the small leadless terminals and large, comparatively, SMT pads. Fine Line Stencil has developed proven formulas that calculate the required volume increase eliminate the insufficient solder volume problem without causing bridging. The recommended stencil aperture size is as follows:

QFN 20-pin: 0.009" x 0.0355" (10.5% volume increase)
(blue = SMT pad, red = IC foot, magenta = recommended stencil aperture, green = drill)

To minimize voids in the thermal pad, the four vias are not pasted. Applying solder paste around, but no directly over, the open vias minimizes the amount of flux and solder that gets lost to the via barrels. Voids in thermal pads with open vias are common not due to trapped gases, but insufficient solder volume. Not printing directly over the vias retains more of the solder volume for the joint between the PCB and component thermal pads.

0603 and 0805 Chips

The 0603 and 0805 land pads are too far apart for the sizes of the chip packages. Any shift at pick-and-place can cause tombstone problems at reflow. To eliminate the tombstone potential, solder paste was removed from the back end of the chips. This will lower the wetting strength at the ends of the terminals and reduce the downward pull on the chip terminals. When one terminal has a much larger downward pull, due to more solder paste wetting to the terminal, the chip can be tipped onto its end causing it to tombstone.



(blue = SMT pad, red = chip package and terminals, magenta = recommended stencil aperture)